In The Specification:

Please replace paragraph [0052] with the following amended paragraph:

[0052] Figure 9 shows another embodiment of a non-gated STI-blocking diode. In Figure 9, the SOI non-gated diode is formed on a SOI substrate that comprises a substrate 90, an insulating layer 92 and a silicon layer. The substrate 90 includes a P- or an N- substrate, while the insulating layer includes a buried oxide layer. The SOI non-gated STI-blocking diode is formed in the silicon layer. In the silicon layer, the SOI diode is formed between two STI structures 94. That is, the doped regions of the SOI diode are isolated by two STI structures. On the insulating layer 92 and between the STI structures, ~~two neighboring lightly doped P-type and N-type doped regions~~ a lightly doped P-type region and a lightly doped N-type region directly connected to the lightly doped P-type region (P- well region 98b and N- well regions 98a) are formed. In addition, heavily doped P+ diffusion region 96b ~~and N+ diffusion region 96a are~~ is formed between the STI structures 94 and the P- well region ~~and N- well region~~ 98b, ~~98a,~~ and heavily doped N+ diffusion region 96a is formed between the STI structures 94 and the N- well region 98a. The difference between this embodiment and Figure 2 includes that the PN junction of the SOI non-gated diode is located in the middle of the whole structure, while the PN junction in Figure 2 is located at the edge.